REMARKS

Claims 1-6, 8-15, and 18 are pending in the application. By this Amendment, claims 1 and 8 have been amended and claim 7 has been cancelled. Exemplary support for the amendments can be found at least in the original claims and specification. (See, for example, cancelled claim 7; Page 3, lines 7-8 of the specification). Therefore, no new matter has been added.

Applicants respectfully request the Examiner to reconsider and withdraw the outstanding rejections in view of the foregoing amendments and the following remarks.

Claim Rejections under 35 U.S.C. § 103(a)

The Office Action rejects claims 1-15 and 18 under 35 U.S.C. § 103(a) as allegedly unpatentable over U.S. Pre-Grant Publication No. 2004/0077156 ("Tsakalakos") in combination with U.S. Pre-Grant Publication No. 2003/0010971 ("Zhang"). The rejection is respectfully traversed.

Initially, it should be noted that M.P.E.P. § 2142 provides that "to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Furthermore, if an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending

therefrom is nonobvious. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

(i) Presently Pending Amended Independent Claim 1

It should be noted that presently only one independent claim is pending - claim 1. Claims 2-6, 8-15, and 18 directly or indirectly depend from amended independent claim 1.

The presently pending amended independent claim 1 recites a method of manufacturing a semiconductor device, the method comprising: (a) **sequentially stacking a semiconductor layer, a mask layer, and a metal layer on a substrate**; (b) anodizing the metal layer to transform the metal layer into a metal oxide layer including a plurality of nanoholes; (c) etching the mask layer using the metal oxide layer as an etch mask until the nanoholes are extended to the surface of the semiconductor layer; (d) removing the metal oxide layer by etching; and (e) **regrowing the semiconductor layer to completely fill nanoholes in the mask layer and extend above the mask layer and cover the mask layer between nanoholes**, wherein **the semiconductor layer is formed of a nitride semiconductor**.

(ii) Tsakalakos

Tsakalakos relates to reducing the dislocation density in an overgrown film by patterning nanoscale features in a semiconductor layer. (Page 1, paragraph [0002]). Tsakalakos discloses a method of fabricating a semiconductor film, comprising: providing a substrate material compatible with the growth of a semiconductor layer;

depositing an inorganic mask layer directly onto the substrate; depositing a block copolymer film onto the inorganic mask layer; etching the block copolymer film to leave an array of nanoscale features; etching the underlying inorganic mask layer to leave the array of nanoscale features; and growing the semiconductor film on exposed areas of the substrate epitaxially within the nanoscale features. (See claim 3 of Tsakalakos).

Tsakalakos does not disclose or suggest **sequentially stacking a semiconductor layer, a mask layer, and a metal layer on a substrate**. Tsakalakos instead describes a substrate having an inorganic mask layer directly deposited on the substrate. (Page 2, paragraph [0027]). Furthermore, Tsakalakos does not disclose or suggest a metal layer which is formed on the mask layer.

Applicants further respectfully submit that Tsakalakos fails to disclose or suggest (b) anodizing the metal layer; (c) etching the mask layer using the metal oxide layer as an etch mask until the nanoholes are extended to the surface of the semiconductor layer; (d) removing the metal oxide layer by etching. Tsakalakos also fails to disclose or suggest (e) **regrowing the semiconductor layer to completely fill nanoholes in the mask layer and extend above the mask layer and cover the mask layer between nanoholes**.

Additionally, the block copolymer nanolithography disclosed by Tsakalakos at page 3, paragraphs [0028]-[0034], is not the same as or interchangeable with the presently recited step of etching the mask layer using the metal oxide layer as an etch mask.

As such, Applicants respectfully submit that Tsakalakos does not disclose or suggest the combination of features presently recited in amended independent claim 1.

(iii) Zhang

Zhang relates to methods of forming integrated circuit devices and device formed thereby and, more particularly, to methods of forming integrated circuit devices having nano-scale features therein and integrated circuit devices formed thereby. (Page 1, paragraph [0003]). Referring to FIGS. 5A-5F, Zhang discloses a method which includes growing an N-type $Al_xGa_{1-x}As$ layer on an underlying compound semiconductor substrate gallium arsenide (GaAs). A silicon dioxide layer or other acceptable insulating material layer is then deposited on the $Al_xGa_{1-x}As$. An aluminum metal layer is then formed on the silicon dioxide layer. The aluminum metal layer is subjected to a repeated anodization process to convert the aluminum metal layer into an anodized aluminum oxide (AAO) layer having a closely-packed highly regular array of nanopores therein. (Page 6, paragraphs [0040] and [0041]).

The presently pending amended independent claim 1 recites a method of manufacturing a semiconductor device, the method comprising: (a) sequentially stacking a semiconductor layer, a mask layer, and a metal layer on a substrate; (b) anodizing the metal layer to transform the metal layer into a metal oxide layer including a plurality of nanoholes; (c) etching the mask layer using the metal oxide layer as an etch mask until the nanoholes are extended to the surface of the semiconductor layer; (d) removing the metal oxide layer by etching; and (e) regrowing the semiconductor layer to completely fill nanoholes in the mask layer and

extend above the mask layer and cover the mask layer between nanoholes, wherein **the semiconductor layer is formed of a nitride semiconductor**.

Initially, it should be noted that in FIGS. 5A-5E, Zhang uses the layer 96 as a growth mask template. However, the mask layer 96 is an electrically insulating layer (*e.g.*, SiO_2). *See* page 6, paragraphs [0040] and [0041] of Zhang. The titanium layer on the mask layer 96 is not a growth mask, but only a barrier layer. The titanium metal layer itself cannot be used as a growth mask. In addition, the layer 96 for a growth mask should not be a metal but an insulator. This is because the material of the layer 96 between the channels must have a wide band gap, *i.e.*, a wide enough band gap to treat the lateral coupling of quantum dots 90a, 90b, as negligible. *See* paragraph [0042] of Zhang.

Additionally, Applicants respectfully submit that Zhang does not disclose or suggest that a **semiconductor layer is formed of a nitride semiconductor**.

The Examiner asserts, however, at page 5 of the Official Action dated August 9, 2006 that it would have been obvious to one of ordinary skill in the art to form a GaN based semiconductor in Zhang. Applicants respectfully disagree with the Examiner's position for the following reasons.

Tsakalakos' GaN is not necessarily interchangeable with Zhang's $Al_xGa_{1-x}As$. However, it is asserted on page 5 of the Official Action dated August 9, 2006 that Tsakalakos' GaN is interchangeable with Zhang's $Al_xGa_{1-x}As$ because the purpose of both inventions is to form nanoholes in the mask and then grow compound semiconductor based layer on the mask with nanoholes to reduce defects or dislocations.

According to this reasoning, semiconductor materials are readily interchangeable without regard to the specific demands of various processes. The Official Action has cited no legal authority, technical evidence, or technical reasoning to support this position. The basis for the Examiner's assumption is not provided in the Official Action.

Applicants respectfully submit that GaN is **not** necessarily interchangeable with $Al_xGa_{1-x}As$, especially when various types of $Al_xGa_{1-x}As$ can have significantly different properties depending on the value of x. No technical reasoning has been supplied to assert that GaN will necessarily be equivalent to $Al_xGa_{1-x}As$ generally, much less when x has a particular value such as 0, 1, 2, 3, 4, or 5....

Furthermore, according to M.P.E.P. § 2144.03, if Applicants adequately traverse the Examiner's assertion of official notice, the Examiner must provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 C.F.R. § 1.104(c)(2). See also In re Zurko, 258 F.3d 1379, 1385, 59 USPQ2d 1693, 1697 (Fed. Cir. 2001). If the Examiner is relying on personal knowledge to support the finding of what is known in the art, the Examiner must provide an affidavit or declaration setting forth specific factual statements and explanation to support the finding. See 37 C.F.R. § 1.104(d)(2).

If the Examiner is taking official notice of the fact that GaN is interchangeable with $Al_xGa_{1-x}As$, according to M.P.E.P. § 2144.03, it would not be appropriate for the Examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be

supported by citation to some reference work recognized as standard in the pertinent art. In re Ahlert, 424 F.2d 1088, 1091, 165 USPQ 418, 420-21 (CCPA 1970). See also In re Grose, 592 F.2d 1161, 1167-68, 201 USPQ 57, 63 (CCPA 1979). Moreover, "when the PTO seeks to rely upon a chemical theory, in establishing a prima facie case of obviousness, it must provide evidentiary support for the existence and meaning of that theory." In re Eynde, 480 F.2d 1364, 1370, 178 USPQ 470, 474 (CCPA 1973).

Applicants respectfully submit that obviousness cannot be predicated on what is not known at the time an invention is made, even if the inherency of a certain feature is later established. In re Rijckaert, 9 F.2d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993). See M.P.E.P. § 2141.02.

Applicants further respectfully submit that when an Examiner relies on a scientific theory, evidentiary support for the existence and meaning of that theory must be provided. In re Grose, 592 F.2d 1161, 201 USPQ 57 (CCPA 1979). See M.P.E.P. § 2144.02.

In light of the above, Applicants respectfully submit that there is no basis to "assume" that GaN is interchangeable with $Al_xGa_{1-x}As$ especially when the properties of the semiconductor can drastically vary depending on the value of x.

Moreover, the Examiner's attention is directed to page 5 of the specification, wherein it is provided that where the second semiconductor layer is re-grown by using the mask layer having the nanopattern as a mask, propagation of defects can be prevented using selective growth. Also, if the second semiconductor layer is subsequently re-grown on the nanopattern, abnormal defect distribution can be minimized at an interface between the second semiconductor layer and the

nanopattern, thus maintaining a stable structure of the semiconductor device. (Page 5, lines 5-8 of the specification).

As such, Applicants respectfully submit that Zhang does not disclose or suggest the combination of features presently recited in amended independent claim 1.

(iv) The combination of Tsakalakos and Zhang

Applicants respectfully submit that Zhang does not overcome the many deficiencies of Tsakalakos.

Tsakalakos, as discussed above, at least fails to disclose or suggest **sequentially stacking a semiconductor layer, a mask layer, and a metal layer on a substrate**. Tsakalakos also fails to disclose or suggest **regrowing the semiconductor layer to completely fill nanoholes in the mask layer and extend above the mask layer and cover the mask layer between nanoholes**.

Zhang, as discussed above, at least fails to disclose or suggest that **the semiconductor layer is formed of a nitride semiconductor**. Moreover, as provided hereinabove, the Official Action does not provide any technical reasoning to interchange Zhang's $Al_xGa_{1-x}As$ with Tsakalakos' GaN. As such, there is no basis to "assume" that GaN is interchangeable with $Al_xGa_{1-x}As$ especially when the properties of the semiconductor can drastically vary depending on the value of x.

It should further be noted that the block copolymer films of Tsakalakos, which creates the nanoscale patterns, requires only an etching process. To accept the hypothetical combination proposed in the Office Action, one skilled in the art would have to adopt a relatively complex process as disclosed in Zhang. Further,

Applicants respectfully submit that one skilled in the art would not move from a relatively straightforward single step process to a relatively complex multistep process absent some compelling reasons or advantages to be gained, the teaching of which is not present in the applied art.

Stated in a different light, the approach taken by Tsakalakos and Zhang are neither equivalent nor would it be reasonable to assume that one of ordinary skill in the art would opt for the more complex process without their being additional reasons not apparent in the record. In other words, the prior art does not supply motivation for a hypothetical combination which would result in the present application but instead it is respectfully submitted that the Office must have relied on hindsight in reconstructing the Applicants' invention using Applicants' own teachings and claims as a template to pick and choose features from the applied art.

Moreover, as Zhang discloses that its purpose is to create electrical devices in the form of nanoscale metal-oxide-semiconductor field-effect transistors (MOSFETs) in the nanopores it forms, it would be inappropriate to suggest that it would be obvious to one of ordinary skill in the art to find motivation for the hypothetical combination despite the destruction of the core features and function of Zhang.

It should also be noted that as mentioned during the personal interview conducted on June 23, 2006 and repeated in the Amendment of July 21, 2006 at page 7 and in the Amendment of November 9, 2006 at page 7, a problem with a hypothetical combination proposed in the Office Action is that the intended purpose or function of one or both of the applied references is destroyed by their combination. This indicates that a *prima facie* case of obviousness has not been established. In re Gordon, 733 F. 2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984).

In light of the foregoing, Applicants respectfully submit that Tsakalakos and Zhang fail to disclose or suggest the combination of features recited in amended independent claim 1.

As such, Tsakalakos and Zhang fail to disclose or suggest the features recited in claims 2-6, 8-15, and 18 which depend directly or indirectly from claim 1.

Therefore, the obviousness rejection of claims 1-6, 8-15, and 18 should be withdrawn.

Conclusion

Applicants invite the Examiner to contact Applicants' representative at the telephone number listed below if any issues remain in this matter, or if a discussion regarding any portion of the application is desired by the Examiner.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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